

REMARKS

This responds to the Office Action mailed on May 25, 2005.

Claim 1 is amended, and no claims are canceled or added; as a result, claims 1-13 are now pending in this application.

§102 Rejection of the Claims

Response to Rejection of Claims 1 and 5-10:

Claims 1 and 5-10 were rejected under 35 USC § 102(b) as being anticipated by Rai et al. (U.S. 4,818,728). Applicant has amended claim 1, from which claims 5-10 depend, and respectfully traverses the rejection. Amendments to claim 1 are supported in the originally filed application at page 3, line 27 through page 4, line 25.

Rai et al. disclose a method of making a semiconductor device having first and second semiconductor units, where the first and second semiconductor units include semiconductor substrates 1 and 1' (col. 3, lines 63-66 and Fig. 1(C)).

Applicant's claims 1 and 5-10 include at least the following distinguishing features:

"... fabricating a second circuit board having multiple optoelectrical display elements and one or more second bond pads electrically connected to the multiple optoelectrical display elements. . ."

Nowhere do Rai et al. disclose fabricating a second circuit board having multiple optoelectrical display elements and one or more second bond pads electrically connected to the multiple optoelectrical display elements.

Based on the amendment to claim 1 and the above remarks, Applicant believes that the rejection of claims 1 and 5-10 under 35 USC § 102(b) has been overcome. Applicant respectfully requests that the Examiner reconsider and withdraw the rejection, and allow claims 1 and 5-10.

Response to Rejection of Claims 1 and 4-9:

Claims 1 and 4-9 were rejected under 35 USC § 102(b) as being anticipated by DiStefano et al. (U.S. 5,891,446). Applicant has amended claim 1, from which claims 4-9 depend, and respectfully traverses the rejection.

DiStefano et al. disclose a microelectronic assembly, which includes a microelectronic component or chip 20 connected to terminals 26 (Figure 1, col. 5, lines 16-33). The component 20 is attached to contact pads 52 of a substrate or second microelectronic component 50 (Figure 1, col. 7, lines 3-6). Between each terminal 26 and contact pad 52 is a spherical joining unit 28 (Figure 1, lines 22-25). Solder 32 is associated with each joining unit 28, and that solder 32 is bonded to the terminal 26 and joining unit 28 in a first heating process (col. 6, lines 43-55). After alignment of the second component 50, a second heating process is performed to bond contact pad 52 to the solder 32 (col. 7, lines 26-35).

Applicant's claims 1 and 4-9 include at least the following distinguishing features:

“ . . . fabricating a second circuit board having multiple optoelectrical display elements and one or more second bond pads electrically connected to the multiple optoelectrical display elements . . . ”

Nowhere do DiStefano et al. disclose fabricating a second circuit board having multiple optoelectrical display elements, and one or more second bond pads electrically connected to the multiple optoelectrical display elements.

Based on the amendment to claim 1 and the above remarks, Applicant believes that the rejection of claims 1 and 4-9 under 35 USC § 102(b) has been overcome. Applicant respectfully requests that the Examiner reconsider and withdraw the rejection, and allow claims 1 and 4-9.

§103 Rejection of the Claims

Response to Rejection of Claims 2 and 3:

Claims 2 and 3 were rejected under 35 USC § 103(a) as being unpatentable over DiStefano et al. Applicant respectfully traverses the rejection.

Claims 2 and 3 depend from claim 1. As discussed above in conjunction with the response to the rejection of claims 1 and 4-9 under 35 USC § 102(b), Applicant believes that claim 1 is allowable over DiStefano et al..

Because DiStefano et al. neither disclose, suggest or motivate the limitations of Applicant's claims 2 and 3, Applicant believes these claims to be allowable. Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claims 2 and 3 as being unpatentable over DiStefano et al., and that the Examiner further allow these claims.

Response to Rejection of Claims 10-13:

Claims 10-13 were rejected under 35 USC § 103(a) as being unpatentable over DiStefano et al. in view of Marrs (U.S. 5,795,818). Applicant respectfully traverses the rejection.

Claims 10-13 depend from claim 1. As discussed above in conjunction with the response to the rejection of claims 1 and 4-9 under 35 USC § 102(b), Applicant believes that claim 1 is allowable over DiStefano et al. Further, Marrs does not disclose the distinguishing features of Applicant's claim 1, either alone or in combination with DiStefano et al.

Because DiStefano et al. in view of Marrs neither disclose, suggest or motivate the limitations of Applicant's claims 10-13, Applicant believes these claims to be allowable. Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claims 10-13 as being unpatentable over DiStefano et al. in view of Marrs, and that the Examiner further allow these claims.

AMENDMENT UNDER 37 C.F.R. 1.116 – EXPEDITED PROCEDURE

Serial Number: 10/628,594

Filing Date: July 28, 2003

Title: METHOD FOR MANUFACTURING AN INTERCONNECTED CIRCUIT BOARD ASSEMBLY AND SYSTEM

Assignee: Intel Corporation

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Dkt: 884.264US2 (INTEL)

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney Sherry Schumm at (480) 538-1735 or Applicant's below-named representative at (612) 349-9592 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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By their Representatives,

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Date Sept. 27, 2005

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 27th day of September, 2005.

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Signature